MM RFFT–4K – Silicon IP Datasheet

Features and specifications

- Energy efficient dynamically reconfigurable FFT
- Dynamically selectable 64, 128, 256, 512, 1024, 2048 and 4096 point FFTs
- Standalone solution – includes input data memory
- Clock frequencies supported: 40 MHz – 300 MHz on ASIC
- Fully synchronous flow
- Throughput equal to clock rate
- Parallel-pipeline architecture
- FFT computation based upon Radix 4^3 algorithm
- 16- bit fixed point data representation (Q1.15 format)
- Provision for scaling to larger FFT sizes

Applications and use cases

- Digital Signal Processing and Telecommunication systems
- OFDM based wireless systems
- Baseband processing in Software Defined Radio
- Spectrum sensing in Cognitive Radio

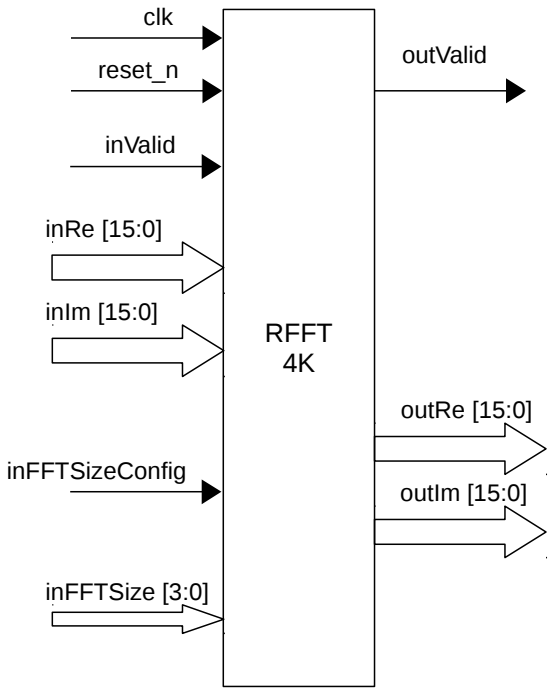
Deliverables

- Synthesizable Verilog RTL source code, or pre-synthesized FPGA netlist, or GDS-II format
- Self-checking testbench including MatLab or GNU Octave based testbench
- Documentation including instructions for integration of the core into ASIC or SoC

Related IPs, solutions, and services

- ***MM LPFFT-64*** – High-performance low-power 64-point FFT core
- ***MM RAES*** – AES cryptography IP core portfolio
- Customization and integration support services for incorporating ***MM*** IPs in customer SoCs

MM RFFT–4K schematic



Performance benchmark† (with 65nm Faraday TC library)	
Area	1.101 mm^2
SQNR	62.4 dB for 64-point FFT 51 dB for 4K-point FFT
Max clock frequency	312 MHz
Max throughput	312 MSPS (4.9 Gbps)
Throughput @ 40 MHz	40 MSPS
Power @ 40 MHz	21.6 mW for 64-point FFT 26.3 mW for 4K-point FFT

† Representative configuration. Custom configurations to suit specific requirements are available

Information on ***Morphing Machines*** and its technologies is overleaf. More information on ***Morphing Machines*** technology, IPs, products, solutions, and services is available at ***http://morphingmachines.com***

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Design Details – Pin Descriptions

Pin	Description	Pin	Description
clk	Clock signal	reset_n	Active low synchronous reset signal
inValid	Data at real and imaginary inputs are valid	inFFTSizeConfig	Active high configuration mode signal
		inFFTSize [3:0]	FFT size: 0 : 64 points 1 : 128 points 2 : 256 points 3 : 512 points 4 : 1,024 points 5 : 2,048 points 6–15 : 4,096 points
inRe [15:0]	16-bit real part of 32-bit complex input	inIm [15:0]	16-bit imaginary part of 32-bit complex input
outRe [15:0]	16-bit real part of 32-bit complex output	outIm [15:0]	16-bit imaginary part of 32-bit complex output
outValid	Data at real and imaginary outputs are valid		

† Flexible, compact, and efficient data interface translator IPs are available to easily adapt input or output data on any I/O bus of arbitrary width to the internal data width of the MM IP cores.

About Morphing Machines

- ***Morphing Machines Pvt Ltd*** is a closely held fabless semiconductor company launched from the Technology Entrepreneurship Initiative of the ***Indian Institute of Science*** at Bangalore, India
- Emerging as one of India's most exciting cutting- edge IP focused technology start-up companies, ***Morphing Machines*** featured as one of the four global start-up semiconductor companies in the ***Cool Vendors 2011*** report of ***Gartner Research***
- Founded by a group of distinguished IIT and IISc alumni with decades of rich experience at world- leading semiconductor, computer, communication, and software technology corporations
- Working in close collaboration with research groups at th***e Indian Institute of Scien***ce at Bangalore, ***Morphing Machines*** has created an exciting portfolio of ***reconfigurable silicon cores***

Technologies and Key IPs

- ***REDEFINE*** – Platform for design and realization of runtime reconfigurable ***Massively Parallel Processor*** and ***Heterogeneous Multicore Processor*** hardware accelerators and SoCs supported by the parallelizing ***REDEFINE C Compiler***
- Breakthrough solutions in multi- protocol ***cryptography, numerical computation,*** and other domains
- ***REDEFINE XNOC*** – Scalable high-performance deadlock-free ***Network-on-Chip*** framework with reconfigurable topologies and multiple interfaces for rapid realization of complex SoCs
- ***MM RAES, MM RECC, MM SHARC*** – Optimized IPs for strong AES encryption / decryption, elliptic curve cryptography, and secure hash functions
- ***MM FPUX*** – High-performance floating-point unit IP supporting multiple precisions and special functions

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